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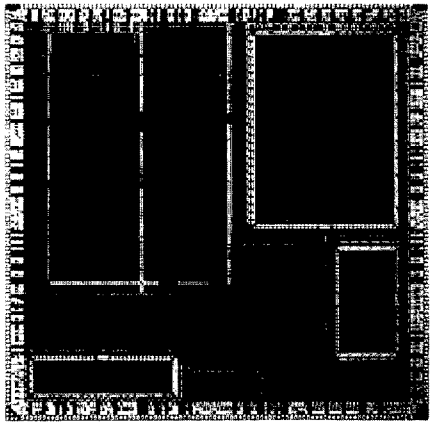
LR33000 Self-Embedding Processor

Introduction

The LSI Logic LR33000 Self-Embedding™ Processor is a 32-bit RISC (Reduced Instruction Set Computer) microprocessor that has been optimized for use in high-performance embedded applications. The LR33000's CPU core is instruction-set compatible with the MIPS-1 architecture, and the LR33000 includes several features on-chip that significantly increase performance, reduce system component count, and ease the overall system design task.

The MIPS-1 architecture incorporates traditional RISC elements such as instruction pipelining, a register-to-register instruction set, and a large, general purpose register file. In addition, the LR33000 has on-chip data and instruction cache memories, which provide a Harvard memory architecture. Separate instruction and data caches allow the LR33000 to perform a data access and fetch an instruction in a single processor cycle. A load or store operation costs most RISC designs several cycles, which significantly raises the average number of cycles per instruction. The LR33000's greater efficiency allows it to provide higher levels of performance than other RISC machines, even those that run at higher clock rates.

In addition to its cache memories, the LR33000's on-chip features include a DRAM controller, three timer/counters, enhanced debug support, and a simple I/O interface, all features that are commonly required in embedded applications.



LR33000 Die

This combination of a MIPS-compatible CPU core and a high level of integration provides a processor that can execute up to 35 MIPS (million instructions per second) at 40 MHz and that is especially suited for embedded applications.

Features

- RISC architecture
  - MIPS-1 instruction set
  - Single-cycle instruction execution
  - LR2000 and LR3000 binary compatibility for user software
- High on-chip integration
  - Eight-Kbyte instruction cache
  - One-Kbyte data cache
  - Three timer/counters
  - DRAM controller
  - One-word-deep write buffer
- Simple I/O interface
  - Direct interface to industry-standard DRAMs
  - Eight- and 32-bit wide boot PROM support
  - Direct interface to other memories and peripherals
  - Direct memory access (DMA) support
  - Programmable wait-state generator
- Simple 1X clock input
- Enhanced debug capability
  - Hardware breakpoint registers
  - Instruction trace capability
- High performance implementation
  - Five-stage pipeline
  - Efficient handling of pipeline stalls and exceptions
  - Both caches accessible during a single CPU cycle
- Strong integrated software support includes high performance optimizing compilers for C, Pascal, FORTRAN, Ada, Cobol, and PL/1
- Development systems available to support native hardware, software, and applications design
- Low power static CMOS design
- Available in 25-, 33-, and 40-MHz versions
- Available in two packages
  - 160-pin Metal Quad Flat Package (MQUAD)
  - 155-pin Ceramic Pin Grid Array (CPGA)

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LR33000 Self-Embedding Processor

Block Diagram

The LR33000 provides several features that especially suit it for embedded applications. Figure 1 is a block diagram of the processor; descriptions of the blocks follow.

MIPS CPU – The LR33000 implements the high-performance MIPS architecture.

- **Instruction Set Compatibility** – The LR33000 maintains full binary compatibility with the R2000 and R3000 microprocessors.
- **Efficient Pipelining** – The CPU's five-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptional events are handled precisely and efficiently.
- **Full 32-bit Operation** – The LR33000 contains thirty-two 32-bit registers. All instructions and addresses are 32 bits wide to provide a 4-Gbyte address space.
- **Enhanced Debug Features** – The LR33000 incorporates hardware breakpoint on program counter and data address registers to ease software debugging, and it incorporates program trace logic.

On-Chip Cache Memory – The LR33000 contains a large 8-Kbyte instruction cache and a 1-Kbyte data cache. The processor can access both caches during a single clock cycle, which allows the processor to execute one instruction per cycle when executing from cache memory. Both caches employ direct address mapping and support bus snooping to maintain cache coherency. The data cache uses a write-through technique to maintain main memory coherency.

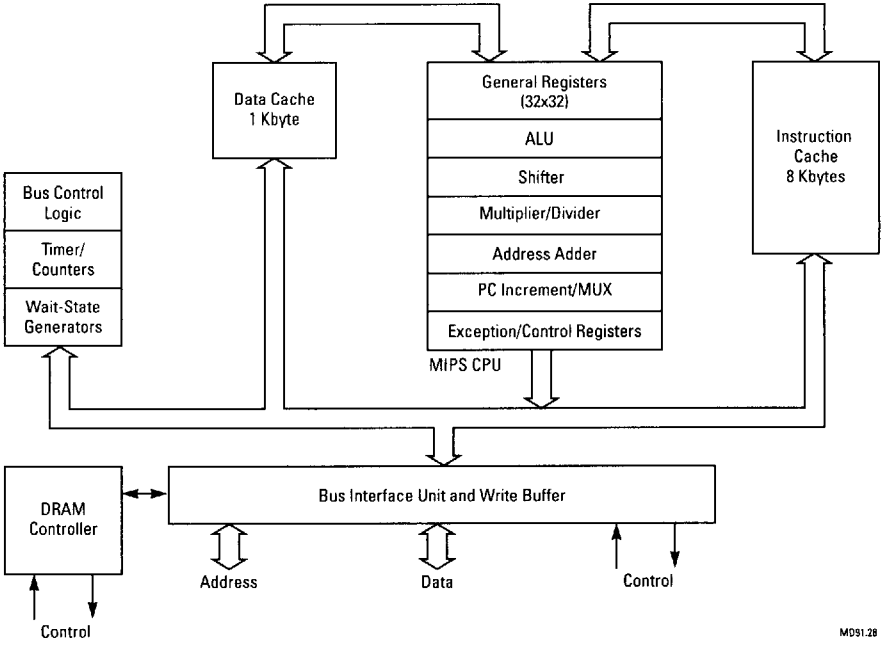

Figure 1. LR33000 Processor Block Diagram

Block Diagram (Continued)

On-Chip DRAM Control – The LR33000 has an integral DRAM Controller that supports most popular DRAMs. Its features include complete support for page-mode DRAMS, CAS-before-RAS refresh, and direct memory access (DMA) by separate I/O devices.

Bus Interface Unit (BIU) – The LR33000's BIU provides a simple memory interface that is easily connected to I/O devices, supports both 8- and 32-bit PROMs and includes programmable wait-state generators. The BIU supports optional parity generation and parity checking. Checking may be suspended on a per-memory-access basis, and the LR33000 provides the PERR output to signal parity errors to external logic.

On-Chip Counter/Timers – The LR33000 includes three counter/timers: two 24-bit general-purpose timers and a 12-bit refresh timer that can support an off-chip DRAM Controller.

MIPS CPU Core

The following subsections describe the essential features of the MIPS CPU Core, including its CPU registers, instruction set, system control processor (CP0), operating modes, and pipeline architecture.

CPU Registers

The LR33000 CPU provides 32 general-purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers (HI and LO). The HI and LO registers hold the results of integer multiply and divide operations. The CPU registers are shown in Figure 2. Notice that the figure does not contain a Program Status Word (PSW) register; the functions traditionally provided by a PSW register are instead provided by the Status and Cause Registers incorporated within the system control coprocessor (CP0).

Instruction Set Overview

All LR33000 instructions are 32 bits long. As shown in Figure 3, instructions have three basic formats: I-type (immediate), J-type (jump), and R-type (register). Instruction decoding is simplified by this approach. More complicated (and less frequently used) operations and addressing modes can be synthesized by the compiler using sequences of simple RISC-type instructions. The assembler recognizes some CISC-type instructions for programming ease, but translates them into sequences of simple instructions.

The LR33000 instruction set is divided into the following groups:

- **Load/Store** instructions are the only instructions that move data between memory and general registers. These instructions are I-type, because the only addressing mode supported is base register plus 16-bit, signed immediate offset.

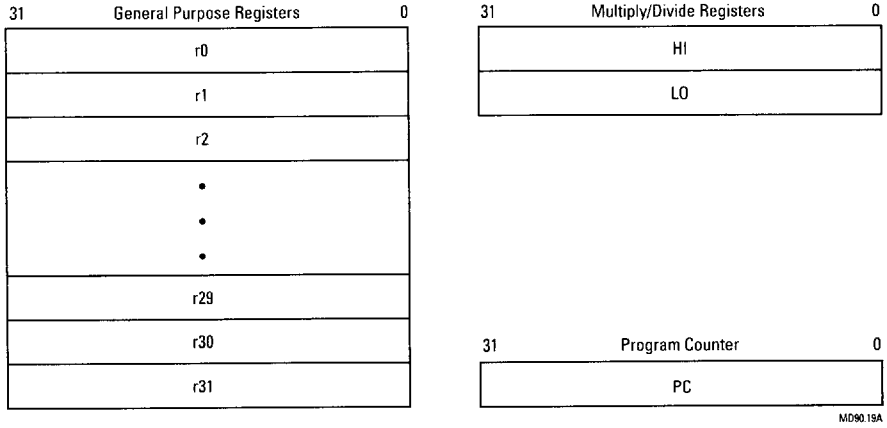

Figure 2. LR33000 CPU Registers

MIPS CPU Core
(Continued)

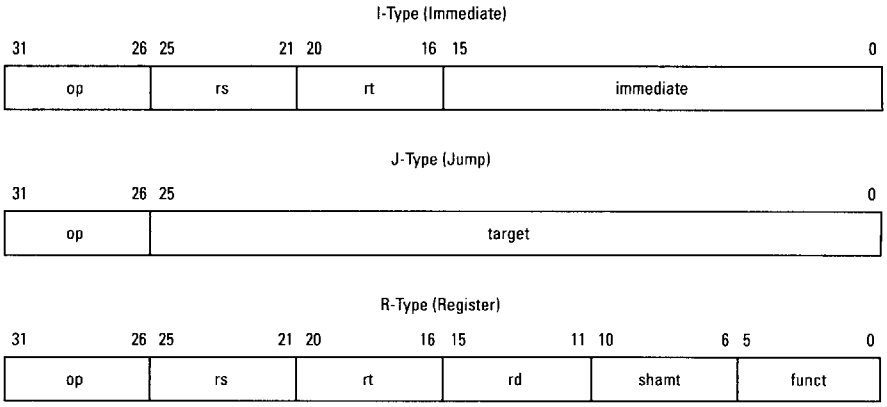

Figure 3. LR33000 Instruction Formats

- **Computational** instructions perform arithmetic, logical, and shift operations on values in registers. These instructions are both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate).
- **Jump** and **Branch** instructions change the control flow of a program. Jumps are always to a paged, absolute address formed by combining a 26-bit target with four bits of the program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in register r31.
- **Coprocessor** instructions perform operations in the coprocessors, most of which are not implemented by the LR33000. See the section entitled "Compatibility with the R2000 and R3000 Microprocessors" on page 10 for details.
- **Coprocessor 0** instructions perform operations on the system control coprocessor (CP0) registers to manipulate the exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks including movement of data between special and general registers, system calls, and breakpoint. These instructions are always R-type.

Table 1 lists the instruction set of the LR33000 processor.

MIPS CPU Core
(Continued)

Table 1. LR33000 Instruction Summary

Op	Description
Load/Store Instructions	
LB	Load Byte
LBU	Load Byte Unsigned
LH	Load Halfword
LHU	Load Halfword Unsigned
LW	Load Word
LWL	Load Word Left
LWR	Load Word Right
SB	Store Byte
SH	Store Halfword
SW	Store Word
SWL	Store Word Left
SWR	Store Word Right
Arithmetic Instructions: ALU Immediate	
ADDI	Add Immediate
ADDIU	Add Immediate Unsigned
SLTI	Set on Less Than Immediate
SLTIU	Set on Less Than Immediate Unsigned
ANDI	AND Immediate
ORI	OR Immediate
XORI	Exclusive OR Immediate
LUI	Load Upper Immediate
Arithmetic Instructions: 3-Operand, Register-Type	
ADD	Add
ADDU	Add Unsigned
SUB	Subtract
SUBU	Subtract Unsigned
SLT	Set on Less Than
SLTU	Set on Less Than Unsigned
AND	AND
OR	OR
XOR	Exclusive OR
NOR	NOR
Shift Instructions	
SLL	Shift Left Logical
SRL	Shift Right Logical
SRA	Shift Right Arithmetic
SLLV	Shift Left Logical Variable
SRLV	Shift Right Logical Variable
SRAV	Shift Right Arithmetic Variable
Multiply/Divide Instructions	
MULT	Multiply
MULTU	Multiply Unsigned
DIV	Divide
DIVU	Divide Unsigned
MFHI	Move From HI
MTHI	Move To HI
MFLO	Move From LO
MTLO	Move To LO
Jump and Branch Instructions	
J	Jump
JAL	Jump And Link
JR	Jump Register
JALR	Jump And Link Register
BEQ	Branch on Equal
BNE	Branch on Not Equal
BLEZ	Branch on Less than or Equal to Zero
BGTZ	Branch on Greater Than Zero
BLTZ	Branch on Less Than Zero
BGEZ	Branch on Greater than or Equal to Zero
BLTZAL	Branch on Less Than Zero And Link
BGEZAL	Branch on Greater than or Equal to Zero And Link
Special Instructions	
SYSCALL	System Call
BREAK	Breakpoint
Coprocessor Instructions	
BCzT	Branch on Coprocessor z True
BCzF	Branch on Coprocessor z False
System Control Coprocessor (CP0) Instructions	
MTC0	Move To CP0
MFC0	Move From CP0
RFE	Restore From Exception

System Control Coprocessor (CP0)

The LR33000's system control coprocessor (CP0) supports exception handling functions of the LR33000. Figure 4 summarizes the register set.

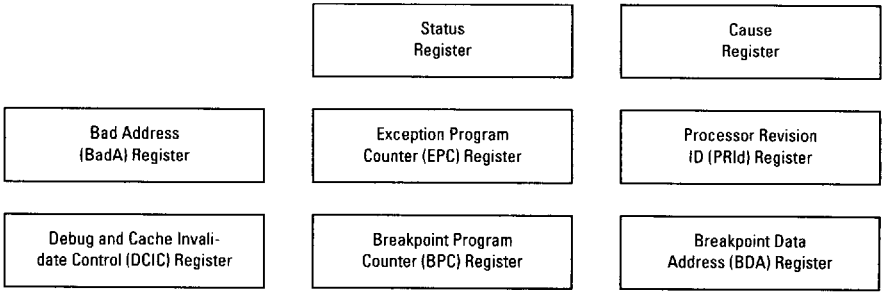

Figure 4. The CP0 Exception-Handling Registers

MIPS CPU Core
(Continued)

Operating Modes

To facilitate the separation of user and supervisory software, the LR33000 has two operating modes: user and kernel. Normally, the processor operates in the user mode until an exception is detected, which forces it into the kernel mode. It remains in the kernel mode until a Restore From Exception (RFE) instruction is executed. Figure 5 shows the address space for the two operating modes.

User Mode – In user mode, a single, uniform address space (kuseg) of 2 Gbytes is available.

Kernel Mode – Four separate segments are defined in kernel mode:

- kuseg – References to this 2-Gbyte segment are treated just like user mode references, thus streamlining kernel access to user data.
- kseg0 – References to this 512-Mbyte segment use cache memory and are hard-mapped to the first 512 Mbytes of memory.
- kseg1 – References to this 512-Mbyte segment do not use the cache and are hard-mapped into the same 512-Mbyte segment of memory space as kseg0.
- kseg2 – References to this 1-Gbyte segment are not mapped and the cacheability of data and instructions is controlled on a per access basis by the $\overline{\text{CACHD}}$ signal.

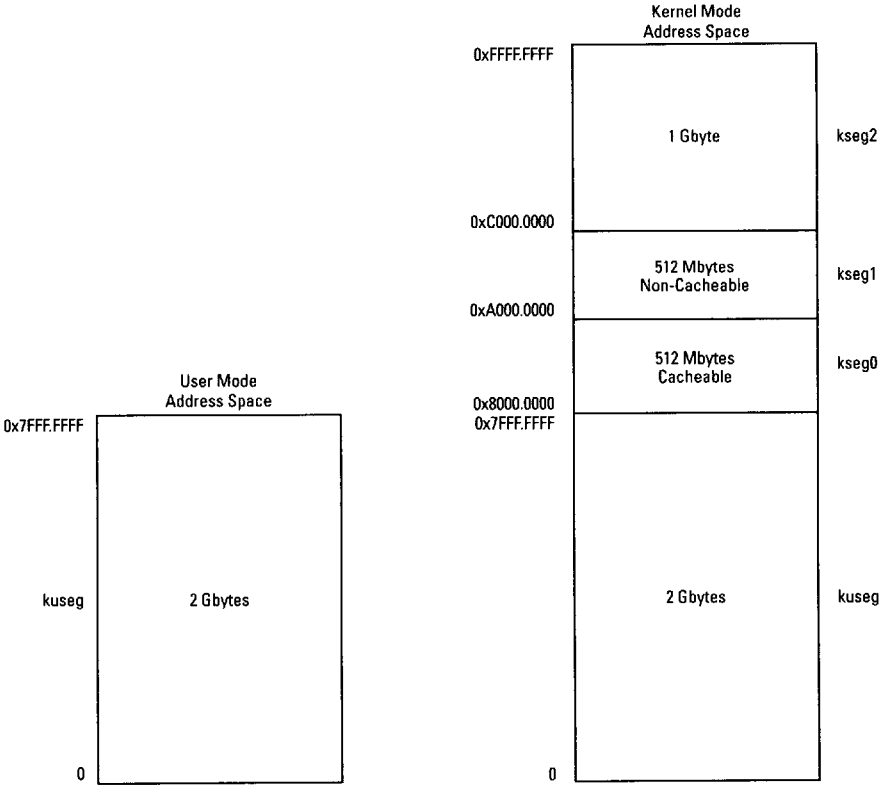

Figure 5. LR33000 Address Space

MIPS CPU Core
(Continued)

Pipeline Architecture

The execution of a single LR33000 instruction consists of five primary steps:

1. **IF** – Fetch the instruction from the instruction cache (I-Cache).
2. **RD** – Read any required operands from CPU registers while decoding the instruction.
3. **ALU** – Perform the required arithmetic or logical operation on instruction operands.
4. **MEM** – Access memory from the data cache (D-Cache).
5. **WB** – Write results back to register file.

Each of these steps requires approximately one CPU cycle as shown in Figure 6 (parts of some operations overlap into another cycle while other operations require only one half cycle).

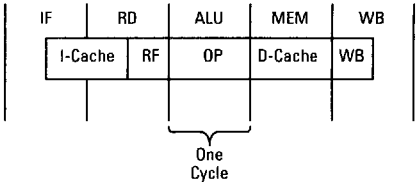

Figure 6. Instruction Execution Sequence

The LR33000 uses a five-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus execution of five instructions at a time are overlapped as shown in Figure 7.

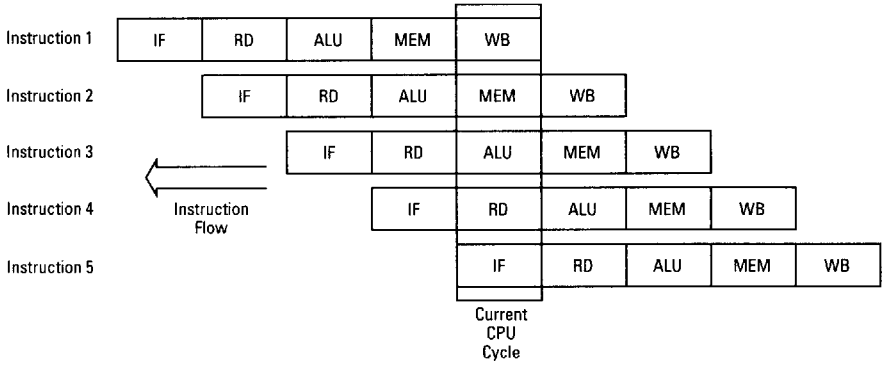

Figure 7. LR33000 Instruction Pipeline

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On-Chip Cache Memories

The LR33000 contains an 8-Kbyte instruction cache and a 1-Kbyte data cache. Both caches are directly mapped to the LR33000's address space. The cache memories hold instructions and data that are repetitively accessed by the CPU (for example, within a program loop) and thus reduce the number of references that must be made to the slower main memory. Although the LR33000's caches are smaller than the caches commonly used for reprogrammable applications, simulations show a 95 percent hit rate for the 8-Kbyte instruction cache, and the ratio of instruction to data cache size (8 to 1) is ideal for most embedded applications.

To provide an additional performance advantage, the LR33000 has separate data and instruction buses to allow the processor to access both caches during a single clock cycle when executing from cache memory. Figure 1 shows the buses. The dual buses allow the processor to execute one instruction per cycle, even during load and store operations.

The LR33000 has several features that ensure coherency between its caches and main memory. The LR33000 uses bus snooping when another system device is performing DMA. During bus snooping, the LR33000 monitors the address bus and when it detects an address that matches the address for a valid entry in the cache, it invalidates that entry to ensure that the data therein does not become stale. To ensure that the main memory is consistent with the data cache, the LR33000 uses a write-through technique. Whenever the LR33000 executes a write and there is a data cache hit, that data is also written through to main memory. In addition to these automatic cache coherency features, software can invalidate cache entries by executing store instructions with the cache invalidate enable bits in the DCIC Register set to one.

The LR33000 supports block refill for both caches. Refill block sizes can be set to 2, 4, 8, or 16 words, and the refill sizes can be set independently for each cache.

On-Chip DRAM Control

The LR33000 has an integral DRAM Controller that supports most popular DRAMs. The DRAM Controller is mapped to a fixed address space of from 0 to 0x0FFF.FFFF, which provides 256 Mbytes of address space for DRAM arrays. For accesses within that address space, the DRAM Controller generates RAS, CAS, OE, and the other control signals necessary to read and write DRAMs. The timing of both the RAS and CAS signals is programmable, and the Controller provides a data ready signal to the processor at the appropriate time in the DRAM access cycle. For small DRAM arrays, the only external logic required is an address multiplexer. Larger arrays require buffers for the control and data signals. Figure 8 shows a simple DRAM system.

When the DRAM Controller is disabled, the DRAM address space can be used to access other types of memory or standard I/O devices.

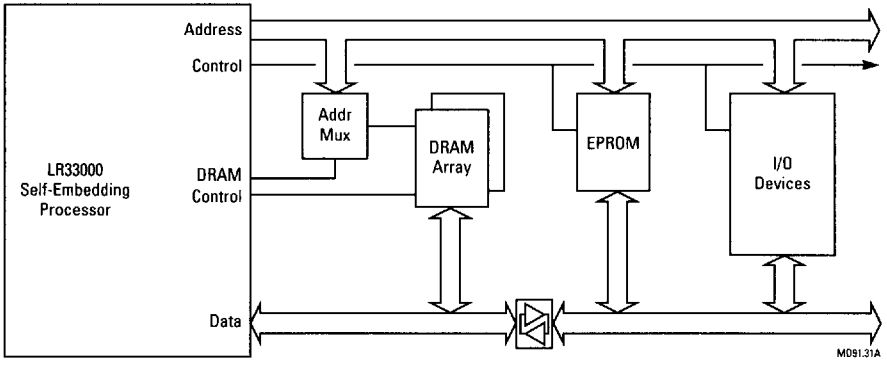


Figure 8. LR33000 Subsystem Interfaces

On-Chip DRAM Control (Continued)

To provide higher system performance, the DRAM Controller utilizes the page mode provided by some DRAMs to support block refills of cache. To provide a further performance boost, the DRAM Controller (with the addition of PAL-implemented control logic) supports interleaved memories.

The DRAM Controller uses the CAS-before-RAS technique to support DRAM refresh. The LR33000 provides a 12-bit Refresh Counter/Timer to signal refresh intervals. The Refresh Counter/Timer can also be used to support external DRAM controllers, and the LR33000's DRAM Controller can be disabled by software.

To provide designers with maximum flexibility, the DRAM Controller supports DMA by external devices and can directly support dual-port DRAMs for those systems that require them.

Bus Interface Unit (BIU)

The LR33000's BIU provides a simple memory interface that is easily connected to I/O devices, supports both 8- and 32-bit PROMs, and includes a programmable wait-state generator. In addition, the BIU includes a one-word-deep write buffer and parity logic.

As shown in Figure 8, the LR33000's memory interface consists of a 32-bit address bus, a 32-bit data bus, a 4-bit parity bus, and the control signals necessary to manage transfers at the interface. The interface is directly compatible with industry standard I/O devices and memory devices such as UARTs, DMA controllers, SRAMs, etc.

I/O Device Support

To make connecting I/O devices to the LR33000 easy, the LR33000 provides an I/O select signal that it asserts for reads or writes in the range 0x1E00.0000 to 0x1EFF.FFFF. The I/O select signal simplifies the address decoders required for I/O devices that are mapped to this range. One of the LR33000's two wait-state generators further simplifies the connection of I/O devices within this address range. When enabled, the wait-state generator stalls the processor for a programmable number of cycles (from 0 to 15). During the last wait state, the wait-state generator asserts the data ready signal, terminating the memory transaction. To accommodate I/O devices of various speeds, software can reprogram the wait-state generator before each access, or faster devices can terminate an access cycle early by asserting the data ready signal before the programmed number of wait states has expired. The LR33000 also supports byte-wide devices by performing byte gathering during reads if an external device asserts the LR33000's BWIDE input.

PROM Support

To make connecting PROMs to the LR33000 easy, the LR33000 provides a PROM select signal that it asserts for reads or writes in the range 0x1F00.0000 to 0x1FFF.FFFF. The LR33000 supports byte-wide devices by performing byte gathering when the LR33000's BWIDE input is asserted. One of the LR33000's two wait-state generators further simplifies the connection of PROMs within this address range. When enabled, the wait-state generator stalls the processor for a programmable number of cycles (from 0 to 15). During the last wait state, the wait-state generator asserts the data ready signal, terminating the memory transaction. To accommodate PROMs of various speeds, software can reprogram the wait-state generator before each access, or faster devices can terminate an access cycle early by asserting the data ready signal before the programmed number of wait states has expired.

The LR33000's bootstrap vector falls within the PROM select signal's address range (0x1F00.0000 to 0x1FFF.FFFF), and the LR33000 maps its exception vectors into the PROM select address range when the Bootstrap Exception Vector (BEV) bit in the Status Register is set to one. The BEV bit is automatically set to one on reset and power-up.

Write Buffer

To eliminate processor stalls during write accesses, the LR33000 includes a one-word-deep write buffer. The write buffer captures data (and the associated address) output by the processor and ensures that the data are passed on to main memory. If the write buffer is full during a write access, the BIU stalls the processor until the buffer empties.

Parity Logic

The BIU supports optional parity generation and checking. Checking may be enabled on a per-memory-access basis, and the LR33000 provides the PERR output to signal parity errors to external logic.

On-Chip Counter/Timers

The LR33000 has two 24-bit counter/timers, Timer 1 and Timer 2, that software can use to time events. These two decrementing timers are clocked by the system clock, and they may interrupt the processor when they reach zero. When they reach zero, the Timer hardware reloads the counter with the initial value and continues decrementing.

Timer 1 is wire-ORed to Interrupt 0 and Timer 2 is wire-ORed to Interrupt 1. When the Timers decrement to zero, they assert the interrupt signals until software resets the interrupt bits in the appropriate Timer Control Register. To allow software to time external events, Timer 2 has an enable input, Timer-2-Enable, and a timeout signal, Timer-2-Timeout, which toggles each time the counter decrements to zero.

Each Timer is initialized and controlled by two memory-mapped registers: an Initial Count Register and a Control Register.

Compatibility with the R2000 and R3000 Microprocessors

The LR33000 Self-Embedding Processor provides instruction set compatibility with the R2000 and R3000 microprocessors. Therefore, software developed for the R2000 and R3000 can be easily ported to systems based on the LR33000, significantly reducing software development time and resource requirements.

However, the LR33000 does not support external coprocessors and does not implement the R2000/R3000 memory management unit (MMU). In addition, the internal cache memories are managed differently and two hardware breakpoint registers have been added to facilitate software debugging. These differences are further described below.

Coprocessor Support

The LR33000 does not support external coprocessors. To prevent unpredictable results should a coprocessor instruction be decoded, all external coprocessors should be disabled by setting the appropriate coprocessor usability bits in CP0's Status Register to zero. When the coprocessors are disabled in this way, the detection of a coprocessor instruction causes a Coprocessor Unusable Exception. Table 2 lists the unsupported coprocessor instructions.

Table 2. Unimplemented Instructions

Op	Description
Coprocessor Instructions	
LWCz	Load Word from Coprocessor
SWCz	Store Word to Coprocessor
MTCz	Move To Coprocessor[1]
MFCz	Move From Coprocessor[1]
CTCz	Move Control To Coprocessor
CFCz	Move Control From Coprocessor
COPz	Coprocessor Operation
System Control Coprocessor (CP0) Instructions	
TLBR	Read indexed TLB entry
TLBWI	Write Indexed TLB entry
TLBWR	Write Random TLB entry
TLBP	Probe TLB for matching entry

Note:
1. Implemented for CP0 only.

The LR33000 provides four coprocessor condition signals that software can test using the Branch on Coprocessor z True and Branch on Coprocessor z False (BCzT and BCzF) instructions. This facility allows software to poll hardware that is connected to the condition signals. The corresponding coprocessor must be enabled to use the test instruction.

Memory Management Unit Support

The LR33000 does not implement the R2000/R3000 memory management unit, which includes the Translation Lookaside Buffer (TLB). Consequently, the LR33000 does not implement any of the instructions designed to maintain and use the TLB. If the processor detects a TLB instruction, it causes a Reserved Instruction Exception. Table 3 lists the unimplemented instructions. In addition, the LR33000 does not implement the TLB registers in CP0: EntryHi, EntryLo, Index, Random, and Context. References to those registers cause a Reserved Instruction Exception.

The System Control Processor: CP0

In addition to the removal of the TLB registers, the LR33000's implementation of CP0 includes additional debug and control registers, which are summarized in Figure 4 on page 5.

Debug Registers – The LR33000 includes program counter and data address breakpoint registers to simplify software debugging. These registers have been incorporated into CP0, and software accesses them using Move from Coprocessor and Move to Coprocessor (MFC0 and MTC0) instructions.

Debug and Cache Invalidate Control Register – This register contains the enable and status bits for the LR33000's debug mechanism and the control bits for the Cache Controller's invalidate mechanism. (The LR33000 does not implement the R2000/R3000 cache control bits, which are located in the Status Register.)

Signal Definitions

This section describes the signals that comprise the LR33000's bit-level interface to other devices. This section is divided into five sections:

- Memory Interface Signals
- Bus Arbitration Signals
- Peripheral Interface Signals
- Status Signals
- Miscellaneous Signals

Memory Interface Signals

This section describes the LR33000's memory interface, which consists of a 32-bit Address Bus, a 32-bit Data Bus, and the control signals required to regulate transactions with memory and I/O subsystems. The memory interface also contains the signals required to control DRAM arrays directly.

A[31:0]
Address Bus [31:0] – When it is bus master, the LR33000 uses A [31:0] to transmit instruction and data addresses to the memory and peripherals. When another device owns the bus, the LR33000 snoops addresses generated by the bus master (if $\overline{\text{CACHD}}$ is asserted).

$\overline{\text{AS}}$
Address Strobe – $\overline{\text{AS}}$ indicates that a valid address is present on the Address Bus. During memory transactions as bus master, the LR33000 asserts $\overline{\text{AS}}$ one half cycle after it asserts $\overline{\text{MXS}}$.

$\overline{\text{BERR}}$
Bus Error – External logic asserts this signal to indicate that an exceptional condition has occurred. When $\overline{\text{BERR}}$ is asserted, the LR33000 terminates the current memory transaction and takes a Bus Error Exception.

BFREQ
Block Fetch Request – The LR33000 asserts this signal to indicate that it wants to perform a block-fetch transaction. The LR33000 asserts BFREQ whenever a cache miss occurs.

$\overline{\text{BFTCH}}$
Block Fetch – In response to the LR33000's assertion of BFREQ, external memory control logic asserts this signal to indicate that the LR33000 can expect a block transfer from memory.

When the LR33000's DRAM Controller is used to manage memory, the DRAM Controller acknowledges the BFREQ signal internally and automatically. Unless there is an external device that is capable of block-fetch transactions, $\overline{\text{BFTCH}}$ should be tied to VDD when using the internal DRAM Controller.

$\overline{\text{BWIDE}}$
Byte-Wide Port – External logic asserts $\overline{\text{BWIDE}}$ to indicate that the memory interface is eight bits wide. When $\overline{\text{BWIDE}}$ is asserted, the LR33000 executes four memory cycles with sequential byte addresses, beginning with the effective address. (The byte-wide feature supports partial-word accesses, but always performs four memory cycles.) If the effective address is not modulo four, the LR33000 wraps around to get all of the bytes in the word in which the effective address falls.

For byte-wide transactions, the LR33000 always takes data from bits D[7:0].

$\overline{\text{CACHD}}$
Cacheable Data – External logic asserts this signal to indicate that the instruction or data fetched during the current cycle may be stored in the LR33000's on-chip cache. If $\overline{\text{CACHD}}$ is not asserted, the LR33000 does not cache the instruction or data fetched during the current transaction.

D[31:0]
Data Bus [31:0] – The LR33000 uses D[31:0] to transfer data and instructions to and from memory and peripherals. When another device owns the bus, it may drive or sample these signals.

$\overline{\text{DCAS}}$
DRAM Column Address Strobe – During a DRAM memory transaction, the LR33000's DRAM Controller asserts this signal to indicate that the address presented to the DRAM array is the column address.

DMXS
DRAM Mux Select – The LR33000's DRAM controller outputs DMXS for the Data Select input of the multiplexers required to multiplex the row and column address from the Address Bus onto the DRAMs' address bus. When HIGH, DMXS indicates that the row address should be selected. When LOW, DMXS indicates that the column address should be selected.

$\overline{\text{DOE}}$
DRAM Output Enable – The LR33000's DRAM Controller asserts this signal to enable DRAM data outputs.

Signal Definitions (Continued)

DP[3:0]
Data Parity [3:0] – DP[3:0] allow the LR33000 to check and transmit parity bits for the four data bus bytes. The LR33000 uses even parity.

$\overline{\text{DRAS}}$
DRAM Row Address Strobe – During a DRAM memory transaction, the LR33000's DRAM Controller asserts $\overline{\text{DRAS}}$ to indicate that the address presented to the DRAM array is the row address.

$\overline{\text{DRDY}}$
Data Ready – External logic asserts this signal to indicate that it can accept or is providing data. The assertion of $\overline{\text{DRDY}}$ terminates the memory transaction. Because the LR33000 must wait for external logic to assert $\overline{\text{DRDY}}$ before it can complete a memory transaction, slow devices can use $\overline{\text{DRDY}}$ to stall the processor. However, when the automatic wait state generator is enabled, the LR33000 asserts an internal version of $\overline{\text{DRDY}}$ to end transactions.

$\overline{\text{EPSEL}}$
EPROM Select – The LR33000 asserts this signal to indicate that it is accessing the $\overline{\text{EPSEL}}$ address space (0x1F00.0000 to 0x1FFF.FFFF). $\overline{\text{EPSEL}}$ can be used as a chip select. If automatic wait state generation is enabled, the LR33000 generates an internal $\overline{\text{DRDY}}$ signal a programmable number of cycles after the transaction begins. The external PROM logic may override the internal wait-state generator by asserting the $\overline{\text{DRDY}}$ signal before the programmed number of wait states have passed.

$\overline{\text{IOSEL}}$
I/O Select – The LR33000 asserts this signal to indicate that it is accessing the $\overline{\text{IOSEL}}$ address space (0x1E00.000 to 0x1EFF.FFFF). $\overline{\text{IOSEL}}$ can be used as a chip select. If automatic wait state generation is enabled, the LR33000 generates its own $\overline{\text{DRDY}}$ signal a programmable number of cycles after the transaction begins. The external I/O logic may override the internal wait-state generator and use the $\overline{\text{DRDY}}$ signal to control the number of wait states.

$\overline{\text{MXS}}$
Memory Transaction Start – The LR33000 asserts $\overline{\text{MXS}}$ for one clock cycle at the beginning of a memory transaction to indicate the start of the transaction.

$\overline{\text{PEN}}$
Parity Enable – When asserted by external logic during a read transaction, the LR33000 performs byte-wise checking for even parity on the Data and Data Parity Buses. When deasserted, the LR33000 does not check parity. External logic that is connected to the LR33000's byte-wide port should never assert $\overline{\text{PEN}}$.

PERR
Parity Error – The LR33000 asserts PERR to indicate that it has detected a parity error during the just-completed memory transaction. PERR can be tied to an interrupt input to cause a parity error exception.

$\overline{\text{RD}}$
Read Strobe – When bus master, the LR33000 asserts $\overline{\text{RD}}$ to indicate that the current transaction is a read transaction and that memory may drive data onto D[31:0]. When deasserted, only the LR33000 may drive D[31:0].

When external logic is bus master, it should drive $\overline{\text{RD}}$ as described in the previous paragraph.

$\overline{\text{RT}}$
Read Transaction – When bus master, the LR33000 asserts $\overline{\text{RT}}$ to indicate that the current memory cycle is a read transaction. The LR33000 deasserts $\overline{\text{RT}}$ during write transactions. When the LR33000 is not bus master, the LR33000 monitors this signal to determine whether it should perform cache snooping.

When external logic is bus master, it should drive $\overline{\text{RT}}$ as described in the previous paragraph.

$\overline{\text{WR}}$[3:0]
Byte Write Strobes [3:0] – The LR33000 asserts these signals to indicate that there is valid data on the corresponding segment of the Data Bus.

Bus Arbitration Signals
This subsection describes the LR33000's bus arbitration signals. The LR33000's memory interface is designed to be used as a general-purpose bus, and these signals allow intelligent peripherals to request bus mastership to per-

Signal Definitions (Continued

form DMA operations or access the LR33000's on-chip cache memories.

$\overline{\text{BREQ}}$
Bus Request – External bus masters assert this signal to request control of the Address and Data Buses and the relevant control signals.

BGNT
Bus Grant – The LR33000 asserts this signal to grant control of the memory buses to the requesting device. When BGNT is asserted, the LR33000 3-states the following signals:

D[31:0]	DP[3:0]
A[31:0]	$\overline{\text{MXS}}$
$\overline{\text{AS}}$	$\overline{\text{RT}}$
$\overline{\text{RD}}$	$\overline{\text{DT}}$
$\overline{\text{WR}}$[3:0]	BFREQ

When BGNT is asserted, the requesting bus master can control the 3-state signals.

$\overline{\text{DMAR}}$
DMA Request – External logic asserts this signal to request use of the LR33000's DRAM Controller. The $\overline{\text{DMAR}}$ and $\overline{\text{DMAC}}$ signals are not related to the $\overline{\text{BREQ}}$ and BGNT signals.

$\overline{\text{DMAC}}$
DMA Cycle – The LR33000 asserts this signal to acknowledge the $\overline{\text{DMAR}}$ and to indicate that the DRAM Controller has started the access for the requesting device. During such DMA accesses, the DRAM Controller manages the $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, and DMXS signals. The DMA device must drive the RAM's write strobes, address bus, and data bus; a configuration that requires multiport RAMs.

During DMA operations by other devices, the LR33000 continues to control and use the A[31:0], D[31:0], and DP[3:0]. If both external logic and the LR33000 need to use the DRAM Controller, they take turns, switching control at the end of each memory transaction.

D$TST
Data Cache Access – When this signal is asserted, external logic can read and write the LR33000's data cache. In data cache access mode the external device controls A[31:0], D[31:0], $\overline{\text{AS}}$, and $\overline{\text{RT}}$ signals.

I$TST
Instruction Cache Access – When this signal is asserted, external logic can read and write the LR33000's instruction cache. In instruction cache access mode the external device controls the A[31:0], D[31:0], $\overline{\text{AS}}$, and $\overline{\text{RT}}$ signals.

Peripheral Interface Signals
The LR33000 contains three counter/timers. Two of the three timers can be controlled via the peripheral interface signal described in this subsection.

CPC[3:0]
Coprocessor Condition [3:0] – The four Coprocessor Condition signals, CPC[3:0], carry condition inputs that the LR33000 can separately test using coprocessor branch instructions. Note that the corresponding coprocessor usable bit (Cu[3:0]) in the Status Register must be set in order to test a condition input.

Although the CPC inputs are tested using coprocessor branch instructions, the LR33000 hardware makes no assumptions about the actual source of these signals. Therefore the use of these condition inputs is application-dependent.

INT[5:0]
Interrupt [5:0] – External logic asserts these signals to cause the LR33000 to take an interrupt exception. Note that interrupts are not sampled in any other type of stall cycles. An instruction sees the interrupt only during the ALU pipe-stage. After the assertion of an interrupt and the occurrence of an interrupt exception, the interrupts continue to be sampled to provide a level-sensitive indication of the active interrupt or interrupts. The interrupts are not latched within the processor when an interrupt exception occurs.

The interrupt inputs can be individually disabled or masked by setting the appropriate bit in the LR33000's Status Register.

$\overline{\text{RTO}}$
Refresh Timeout – The LR33000 asserts this signal to indicate that the Refresh Timer has counted down from its preset value to zero. The LR33000 continues to assert $\overline{\text{RTO}}$ until external logic asserts RTACK, but the Counter does not

Signal Definitions (Continued)

stop running: it loads the initial value and continues to count.

When the DRAM Controller is enabled, this signal indicates that a refresh cycle is in progress. When the DRAM Controller is disabled, external DRAM control logic can use the assertion of $\overline{RTO}$ to start a refresh cycle.

RTACK
Refresh Timer Acknowledge – External logic asserts RTACK to indicate that it has completed the refresh operation initiated by the LR33000's assertion of $\overline{RTO}$. The assertion of RTACK causes the LR33000 to deassert $\overline{RTO}$. External logic must assert RTACK for two cycles to guarantee that $\overline{RTO}$ resets.

When the DRAM Controller is enabled, RTACK must be tied LOW.

T2EN
Timer 2 Enable – External logic asserts this signal to enable the operation of Timer 2. Timer 2 counts as long as T2EN is asserted.

T2TO
Timer 2 Timeout – The LR33000 toggles T2TO to indicate that the LR33000's Timer 2 has counted down from its preset value to zero. T2TO is set LOW on cold and warm starts.

Status Signals
The LR33000 generates four signals that indicate its internal state. Those signals are described in this subsection.

BRTKN
Branch Taken – When asserted, this signal indicates that the condition has been met for a branch instruction in the LR33000's pipeline. The LR33000 signals branches during the ALU stage of the pipeline, which is when the control transfer occurs.

DT
Data Transaction – The LR33000 asserts this signal to indicate that the current bus transaction is a data read or write transaction. The LR33000 deasserts this signal to indicate that the current bus transaction is an instruction fetch.

$\overline{STALL}$
Stall – The LR33000 asserts this signal to indicate that it is in a stall state.

TDONE
Test Mode Transaction Done – The LR33000 asserts this signal to indicate that a cache access mode read or write operation is complete.

Miscellaneous Signals
The LR33000 has six miscellaneous inputs, which are described in this subsection.

BENDN
Big Endian – This signal controls the byte ordering of the LR33000. When BENDN is tied HIGH, byte 0 is the most-significant byte (big endian). When BENDN is tied LOW, byte 0 is the least-significant byte (little endian).

$\overline{FRCM}$
Force Cache Miss – When external logic asserts $\overline{FRCM}$, the LR33000 detects a cache miss on the current instruction fetch. This signal is intended for test and in-circuit emulation purposes.

$\overline{HIGHZ}$
High Impedance – When external logic asserts $\overline{HIGHZ}$, the LR33000 3-states all of its outputs. SYSCLK need not be active for $\overline{HIGHZ}$ to 3-state the LR33000 outputs. In addition, $\overline{HIGHZ}$ selects between warm and cold processor starts after reset. When $\overline{HIGHZ}$ and $\overline{RESET}$ are asserted together, the LR33000 executes a cold start after $\overline{RESET}$ is deasserted. When $\overline{RESET}$ is asserted alone, the LR33000 executes a warm start. The DRAM Controller is *not* re-initialized on a warm start.

$\overline{RESET}$
Reset – A LOW-to-HIGH transition of $\overline{RESET}$ initializes the processor and initiates a non-maskable Reset Exception. Driving $\overline{RESET}$ LOW does not halt the processor or cause any other action. Only a LOW-to-HIGH transition of $\overline{RESET}$ initializes the processor.

SYSCLK
System Clock – This signal is the clock input to the processor. It determines the instruction cycle time of the processor.

THIT
Test Hit – The LR33000 asserts THIT during a read of its instruction or data caches to indicate that the cache tags matched the address of the read. This signal is intended for test purposes.

Specifications

This section provides the electrical specifications for the LR33000. Table 3 lists the absolute maximum rating for the LR33000. Operation beyond the limits set forth in this table may impair the useful life of the device.

Table 4 lists the LR33000's recommended operating conditions, Table 5 lists the capacitance of its inputs and outputs, and Table 6 lists the DC electrical specifications for the LR33000.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
VDD	DC Supply	-0.3 to +7	V
VIN	Input Voltage	-0.3 to VDD +0.3	V
IIN	DC Input Current	±10	mA
TSTG	Storage Temperature Range, Metal	0 to +125	°C
TSTG	Storage Temperature Range, Ceramic	-65 to +150	°C

Note:
1. Referenced to VSS.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
VDD	DC Supply, Commercial	+4.75 to +5.25	V
VDD	DC Supply, Military	+4.50 to +5.50	V
TA	Ambient Temperature, Commercial	0 to +70	°C
TA	Ambient Temperature, Military	-55 to +125	°C

Table 5. Capacitance

Symbol	Parameter[1]	Min	Typ	Max	Unit
CIN	Input Capacitance			5	pF
COUT	Output Capacitance			10	pF
CIO	I/O Bus Capacitance			15	pF

Note:
1. Measurement conditions are VIN = 5.0 V, TA = 25 °C and clock frequency = 1 MHz.

Table 6. DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
VIL	Voltage Input LOW		–	–	0.8	V
VIH	Voltage Input HIGH		2.0	–	–	V
VOH	Voltage Output HIGH	IOH = -4.0 mA IOH = -8.0 mA	2.4 2.4	4.5 4.5	– –	V V
VOL	Voltage Output LOW	IOL = 4.0 mA IOL = 8.0 mA	– –	0.2 0.2	0.4 0.4	V V
IIL	Current Input Leakage	VDD = Max, VIN = VDD or VSS	-10	±1	10	µA
IOZ	Current 3-State Output Leakage	VDD = Max, VOUT = VSS or VDD	-10	±1	10	µA
IIPU	Current Input Pull-up	VIN = VSS or 3.5 V	-35	-115	-350	µA
IOZU	Current 3-State Output w/ Pull-up	VIN = VSS or 3.5 V	-2	–	-175	µA
IOSP4	Current P-Channel Output Short Circuit (4 mA Output Buffers)[2]	VDD = Max, VOUT = VSS	-25	-70	-140	mA
IOSP8	Current P-Channel Output Short Circuit (8 mA Output Buffers)[2]	VDD = Max, VOUT = VSS	-50	-140	-280	mA
IOSN4	Current N-Channel Output Short Circuit (4 mA Output Buffers)[2]	VDD = Max, VOUT = VDD	30	75	140	mA
IOSN8	Current N-Channel Output Short Circuit (8 mA Output Buffers)[2]	VDD = Max, VOUT = VDD	60	150	280	mA
IDD	Quiescent Supply Current	VIN = VDD or VSS	–	–	2	mA
ICC	Dynamic Supply Current	VDD = Max, f = 25 MHz VDD = Max, f = 33 MHz VDD = Max, f = 40 MHz	– – –	450 550 600	550 625 700	mA mA mA

Note:
1. Specified at VDD equals 5 V ± 5% at ambient temperature over the specified range.
2. Not more than one output may be shorted at a time for a maximum duration of one second.

Specifications
(Continued)

Table 7 lists the AC electrical specifications for the LR33000, and Figures 9 through 11 are timing waveforms that illustrate the AC timing values.

In the AC specifications, all timing is referenced to 1.5 V, and all output timing assumes 55 pF of capacitive load.

Table 7. AC Timing Values

Parameter		Description	40 MHz		33 MHz		25 MHz		Units
			Min	Max	Min	Max	Min	Max	
13.	t_{SHAV}	SYSCLK+ to Address Valid	–	17	–	20	–	26	ns
14.	t_{SHBRV}	SYSCLK+ to BFREQ Valid[1]	–	15	–	16	–	20	ns
15.	t_{SHBRI}	SYSCLK+ to BFREQ Invalid	–	15	–	16	–	20	ns
16.	t_{SHML}	SYSCLK+ to $\overline{MXS}$ Low	–	15	–	16	–	20	ns
17.	t_{SHRTL}	SYSCLK+ to $\overline{RT}$ Low	–	15	–	16	–	20	ns
18.	t_{SHRTH}	SYSCLK+ to $\overline{RT}$ High	–	14	–	15	–	18	ns
19.	t_{SHDTV}	SYSCLK+ to $\overline{DT}$ Valid	–	15	–	16	–	20	ns
20.	t_{SHDTI}	SYSCLK+ to $\overline{DT}$ Invalid	–	15	–	16	–	20	ns
21.	t_{SLAL}	SYSCLK- to $\overline{AS}$, $\overline{RD}$ Low	–	17	–	20	–	23	ns
22.	t_{SLSL}	SYSCLK- to $\overline{IOSEL}$ or $\overline{EPSEL}$ Low	–	14	–	15	–	18	ns
23.	t_{SLSH}	SYSCLK+ to $\overline{IOSEL}$ or $\overline{EPSEL}$ High	–	14	–	15	–	18	ns
24.	t_{AVASL}	Address Valid to $\overline{AS}$, $\overline{RD}$, $\overline{IOSEL}$, $\overline{EPSEL}$ Low	5	–	5	–	5	–	ns
25.	t_{CSSL}	Control[2,3] Setup to SYSCLK-	4	–	5	–	6	–	ns
25a.	t_{DRSSL}[4]	DRDY Setup to SYSCLK-	8	–	9	–	10	–	ns
26.	t_{CHSL}	Control[3,5] Hold from SYSCLK-	3	–	4	–	5	–	ns
26a.	t_{BEHSL}	$\overline{BERR}$ Hold from SYSCLK-	5	–	6	–	7	–	ns
27.	t_{DSSH}	Data and Parity Setup before SYSCLK+	0	–	0	–	0	–	ns
28.	t_{DHSH}	Data and Parity Hold from SYSCLK+	6	–	7	–	9	–	ns
29.	t_{SHASH}	SYSCLK+ to $\overline{AS}$, $\overline{RD}$ High	–	12	–	13	–	15	ns
30.	t_{AHSH}[6]	Address Hold from $\overline{AS}$, $\overline{RD}$, $\overline{IOSEL}$, $\overline{EPSEL}$ High	0	–	0	–	0	–	ns
30a.	t_{AHWH}[6]	Address Hold from $\overline{WR}$[3:0] High	0	–	0	–	0	–	ns
31.	t_{SHWRV}	SYSCLK+ to $\overline{WR}$[3:0] Valid	–	15	–	16	–	20	ns
32.	t_{SHDV}	SYSCLK+ to Data and Parity Valid	–	19	–	21	–	26	ns
33.	t_{SHWRH}	SYSCLK+ to $\overline{WR}$[3:0] High	–	13	–	14	–	16	ns
34.	t_{WRHDI}[6]	$\overline{WR}$[3:0] High to Data and Parity 3-State	10	–	10	–	10	–	ns
51.	t_{SLRL}	SYSCLK- to $\overline{DRAS}$ Low	–	13	–	14	–	17	ns
53.	t_{ASRL}	Address Setup before $\overline{DRAS}$ Low	5	–	5	–	8	–	ns
54.	t_{SLMSL}	SYSCLK- to $\overline{DMXS}$ Low	–	13	–	14	–	16	ns
55.	t_{SLMSH}	SYSCLK- to $\overline{DMXS}$ High	–	13	–	14	–	16	ns
56.	t_{SLCAL}	SYSCLK+/- to $\overline{DCAS}$ Low	–	13	–	14	–	17	ns
57.	t_{SLOEL}	SYSCLK- to $\overline{DOE}$ Low	–	13	–	14	–	17	ns
58.	t_{SHCAH}	SYSCLK+ to $\overline{DCAS}$ High	–	13	–	14	–	17	ns
59.	t_{SHOEH}	SYSCLK+ to $\overline{DOE}$ High	–	18	–	19	–	20	ns
63.	t_{SLRAH}	SYSCLK- to $\overline{DRAS}$ High	–	12	–	13	–	15	ns

Note:
1. Block-fetch transactions must have one wait-state in the first word of a block fetch. A block-fetch transaction is requested on any read access to cacheable memory after a cache miss.
2. Includes $\overline{BERR}$, $\overline{CACHD}$, $\overline{BWIDE}$, $\overline{PEN}$, and $\overline{DMAR}$. Also includes $\overline{DRDY}$ only for non-DRAM cycles.
3. Once sampled at SYSCLK-, $\overline{BWIDE}$ is ignored until four bytes have been fetched or a bus error has been detected. $\overline{PEN}$ is ignored if $\overline{BWIDE}$ is sampled at SYSCLK-.
4. This parameter is applicable only when an external controller asserts $\overline{DRDY}$ to terminate a DRAM read or write transaction.
5. Includes $\overline{DRDY}$, $\overline{CACHD}$, $\overline{BWIDE}$, $\overline{PEN}$, and $\overline{DMAR}$.
6. This parameter is guaranteed by design and is not tested.

Specifications
(Continued)

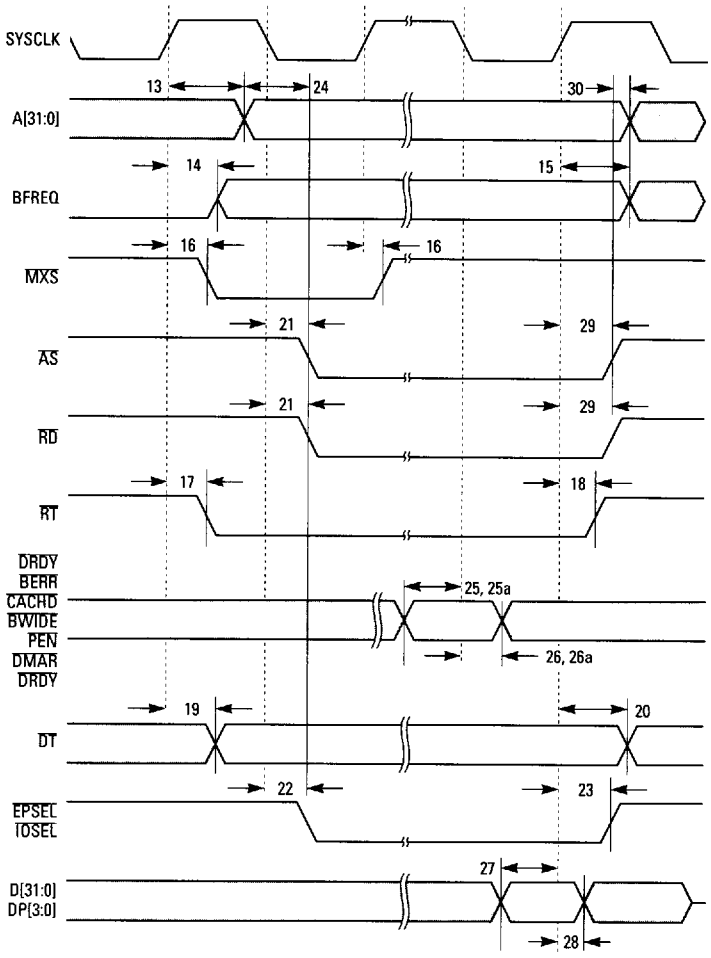


Figure 9. Read Transaction Timing

Specifications
(Continued)

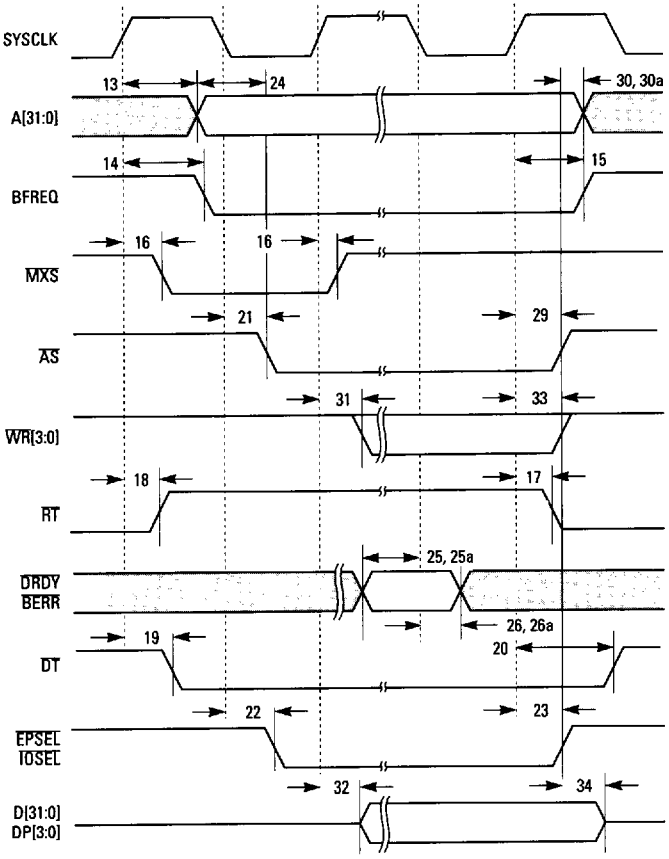


Figure 10. Write Transaction Timing

Specifications
(Continued)

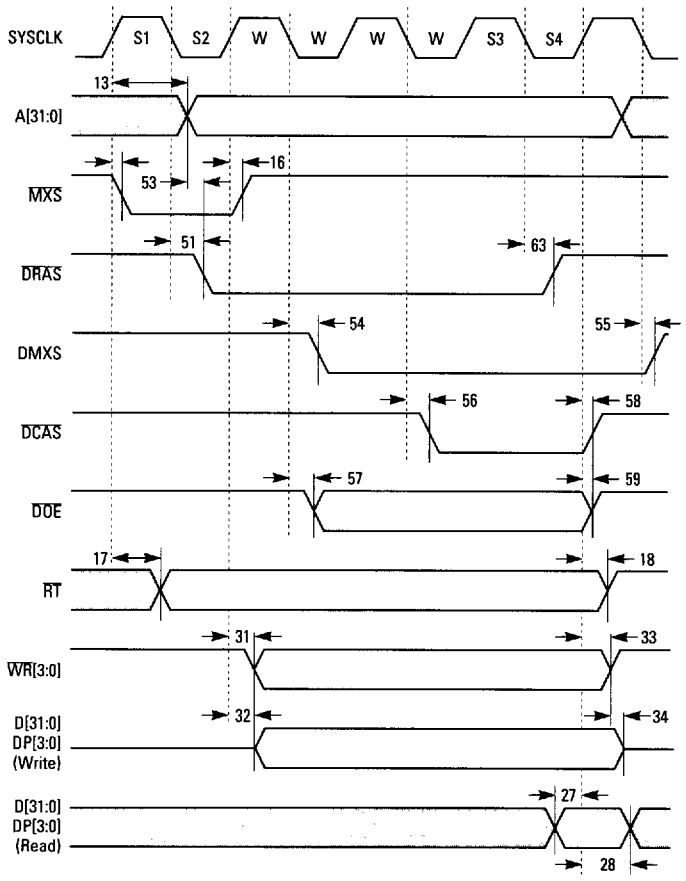


Figure 11. DRAM Access Timing

Pinout, Package, and Ordering Information

The LR33000 is available in two different packages: a 155-pin Ceramic Pin Grid Array (CPGA) and a 160-pin Metal Quad Flat Package (MQUAD). Designers will choose the package that meets the cost and performance requirements of their application.

Table 8 lists and describes the two packages by order number.

This section contains two types of information for each package type: a pinout and a mechanical drawing. For the 155-pin CPGA, Figure 12 and Figure 13 contain the two types of information. For the 160-pin MQUAD, Figure 14 and Figure 15 contain the two types of information.

Table 8. Recommended Operating Conditions

Order Number	Clock Frequency (MHz)	Package Type	Operating Range
LR33000MC-25	25	160-pin MQUAD	Commercial
LR33000MC-33	33	160-pin MQUAD	Commercial
LR33000MC-40	40	160-pin MQUAD	Commercial
LR33000HC-25	25	155-pin CPGA	Commercial
LR33000HC-33	33	155-pin CPGA	Commercial
LR33000HC-40	40	155-pin CPGA	Commercial

Pinout, Package, and Ordering Information (Continued)

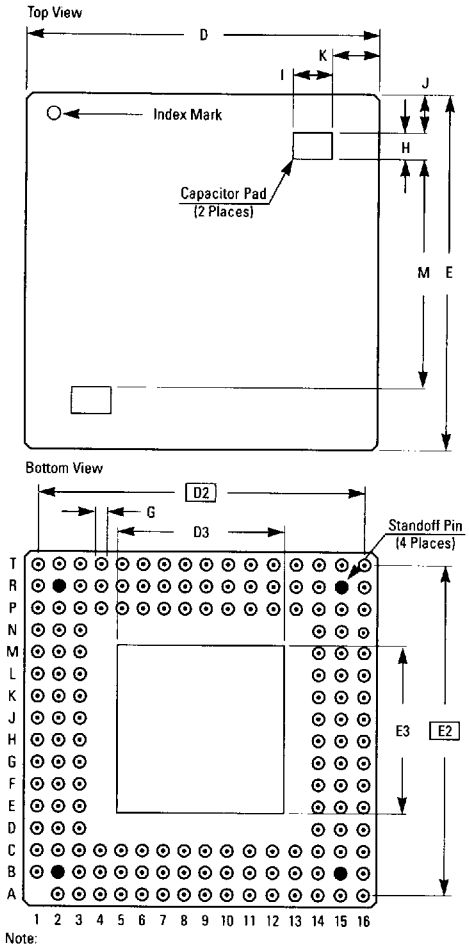
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		VSS	D7	D10	VSS	D14	D17	VSS	VDD	D22	D25	D28	D31	T2TO	VDD	VSS
B	VDD	D6	*	D9	D12	VDD	D16	D19	D20	D23	D26	D29	CACHD	VSS	*	VDD
C	D4	D5	*	D8	D11	D13	D15	D18	D21	D24	D27	D30	PEN	*	PERR	RTO
D	D1	D2	D3											DP0	DP1	DP2
E	*	DMAR	D0											DP3	BFREQ	DOE
F	CPC2	CPC3	TDONE											RD	RT	BREQ
G	BENDN	CPC0	CPC1											BGNT	MXS	DRDY
H	VSS	D$TST	I$TST											AS	BFTCH	VSS
J	VDD	SYSCLK	*					Top View						DCAS	DRAS	VDD
K	STALL	DT	RTACK											WR0	BERR	DMXS
L	T2EN	EPSEL	IOSEL											WR3	WR2	WRT
M	DMAC	HIGHZ	RESET											A0	*	BWIDE
N	INT5	INT4	INT2											A3	A2	A1
P	INT3	FRCM	*	INT1	A29	A26	A23	A21	BRTKN	A16	A13	VDD	A10	A6	A5	A4
R	VSS	*	*	A31	A28	A25	A22	A20	A19	A17	A14	THIT	A11	A8	*	VSS
T	VDD	VSS	INT0	A30	A27	A24	VSS	VDD	VSS	A18	A15	A12	VSS	A9	A7	VDD

MD91.35A

Note:
1. Pins indicated with an asterisk (*) are reserved – do not connect.

Figure 12. 155-Pin CPGA Pinout

Pinout, Package, and Ordering Information (Continued)

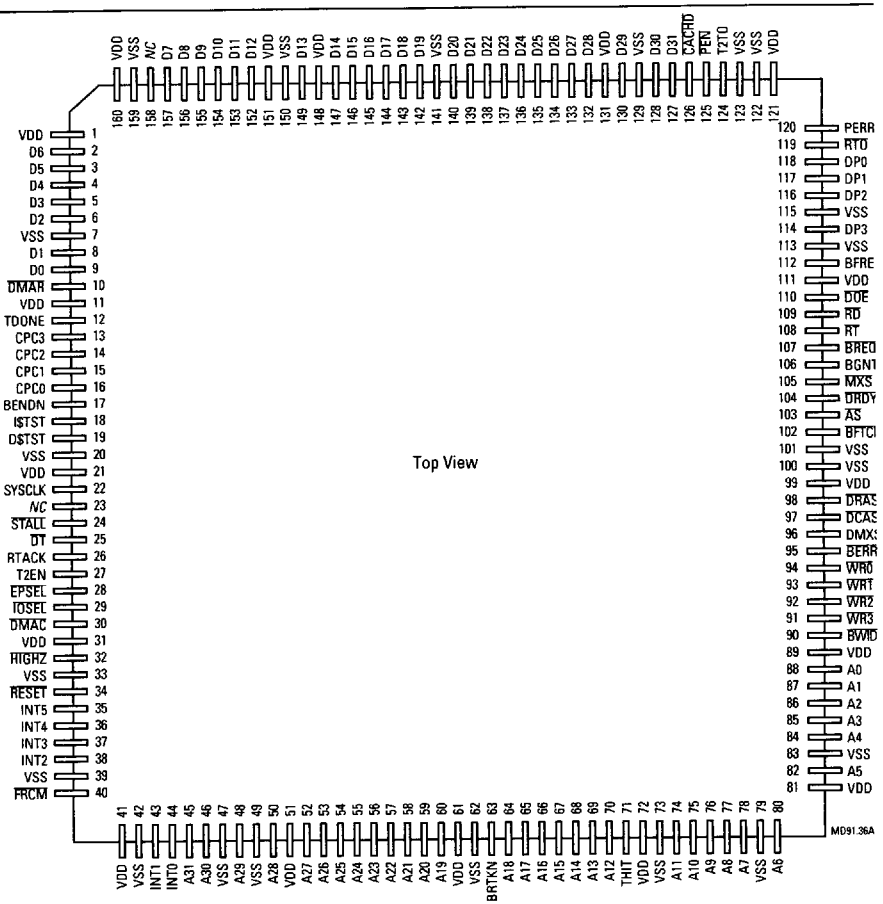


Dimension		Inches
A	Min	0.091
	Nom	0.101
	Max	0.111
A2	Max	0.156
b	Min	0.016
	Nom	0.018
	Max	0.020
b1	Min	0.045
	Nom	0.050
	Max	0.055
b2	Ref	0.008
D	Min	1.643
	Nom	1.660
	Max	1.677
D2	Max	1.500
D3	Ref	0.970
e	Typ	0.100
E	Min	1.643
	Nom	1.660
	Max	1.677
E2	Max	1.500
E3	Ref	0.970
G	Min	0.060
	Nom	0.070
	Max	0.080
H	Max	0.130
I	Max	0.175
J	Ref	0.088
K	Ref	0.115
L	Min	0.185
	Nom	0.190
	Max	0.195
L1	Min	0.065
	Nom	0.070
	Max	0.075
L3	Min	0.020
M	Ref	1.225
N	Max	0.080

Note:
1. Drawing is not to scale.
2. Size of array is 16 x 16. Corner detail and index mark are LSI Logic Corporation options.
3. Total number of pins is 155.
4. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code FR.

Figure 13. 155-Pin CPGA Mechanical Drawing

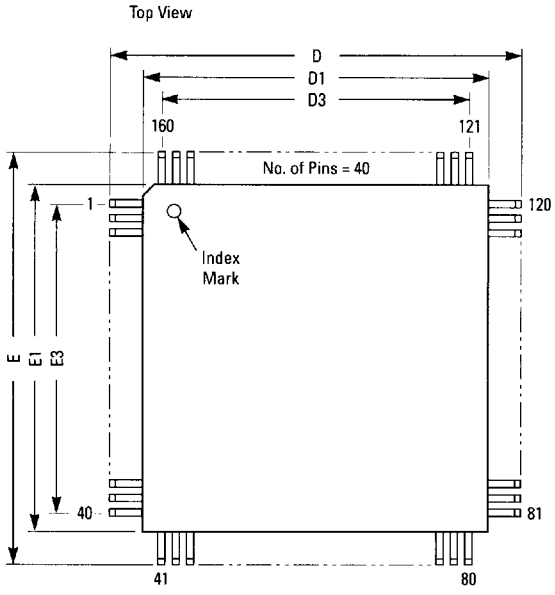
Pinout, Package, and Ordering Information
(Continued)



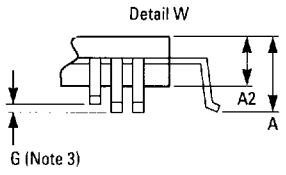
Note:
1. Pins indicated with *NC* are not connected – do not connect.

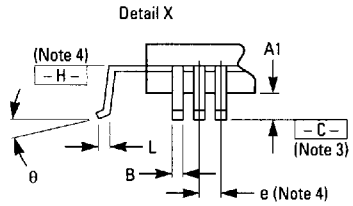
Figure 14. 160-Pin MQUAD Pinout

Pinout, Package, and Ordering Information
(Continued)



Dimension		mm
A	Max	3.68
A1	Min	0.25
	Max	0.51
A2	Min	3.17
	Max	3.43
B	Typ	0.30
D	Min	31.00
	Max	31.40
D1	Min	27.56
	Max	27.72
D3	BSC	25.35
E	Min	31.00
	Max	31.40
E1	Min	27.56
	Max	27.72
E3	BSC	25.35
θ	Min	0°
	Max	7°
e	BSC	0.65
G	Max	0.10
L	Min	0.67
	Max	0.93





Note:
1. Total number of pins is 160.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Lead pitch determined at – H –.
5. Leadframe to package offset tolerance is ±0.10 mm Max.
6. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code WU.

MD93.WU

Figure 15. 160-Pin MQUAD Mechanical Drawing